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Claims

[c1] 1. A method of determining approximately whether a design of a module violates a desired criteria, said design being represented in the form of a data, said method comprising:
examining said data to extract a topology of said design, wherein said topology comprises a plurality of transistors, a plurality of resistors, and a plurality of paths connecting said plurality of resistors and said plurality of transistors;
generating a model of said module by replacing each of said plurality of transistors in said topology by a corresponding one of said plurality of current sources;
computing a magnitude of each of said plurality of current sources by distributing an aggregate amount of current sunk by said module among said plurality of current sources, wherein said magnitude of each current source is treated proportionate to a corresponding width by said computing; and
analyzing said model to determine a corresponding current on each of said plurality of paths,
wherein a determination is made as to whether said design violates said desired criteria based on said corre-

sponding current.

[c2] 2. The method of claim 1, wherein said desired criteria comprises ensuring that a current density on each of said plurality of paths does not exceed a corresponding maximum value, said method further comprising determining whether said corresponding current on each of said plurality of paths corresponds to a current density exceeding said corresponding maximum value.

[c3] 3. The method of claim 2, wherein said desired criteria further comprises ensuring that a voltage drop from a supply voltage to a first node contained in said module is within a corresponding threshold value.

[c4] 4. The method of claim 3, wherein said computing comprises treating said plurality of transistors to be connected in parallel irrespective of said topology of said design.

[c5] 5. The method of claim 3, further comprises rejecting said module if either of said criteria is violated.

[c6] 6. The method of claim 5, wherein said module is comprised in an integrated circuit, said method further comprising performing a chip-level analysis of said integrated circuit, wherein said module is substituted by said model.

[c7] 7. The method of claim 6, wherein said analyzing of said model is performed using a simulation tool.

[c8] 8. The method of claim 3, wherein said data representing said design is provided in the form of a layout file.

[c9] 9. The method of claim 1, wherein said module comprises a memory module containing a memory array, said memory containing a plurality of rows, wherein said topology comprises only a subset of rows of said memory array.

[c10] 10. The method of claim 9, wherein said subset of rows comprises a top row, a bottom row and a middle row.

[c11] 11. The method of claim 10, further comprising determining said top row, said bottom row and said middle row from a layout file representing said memory module, wherein said determining comprises:
examining a special layer of said layout file to determine a coordinate of a gate location of each of a plurality of transistors contained in a memory array of said memory module;
determining boundary coordinates of said memory array based on said coordinates of said gate locations; and
determining a set of transistors in each of said top row, said bottom row and said middle row according to said

boundary coordinates and a height of each of bit cell contained in said memory array.

[c12] 12. The method of claim 9, wherein said generating, said computing and said analyzing are performed in a plurality iterations, wherein a top row of said topology comprises only a top row of said memory array in a first iteration, a middle row of said topology in a second iteration and a bottom row of said memory array in a third iteration.

[c13] 13. A method of analyzing a module to determine whether a plurality of efuse cells contained in a module can be programmed by applying an appropriate voltage level across each of said plurality of efuse cells, wherein one terminal of each of said plurality of efuse cells is connected to a first rail connecting to a first power supply and another terminal of each of said plurality of efuse cells is connected to a second rail connecting to a second power supply, wherein said module is represented in the form of a data, said method comprising: examining said data to extract said plurality of efuse cells and a plurality of resistance networks, wherein said plurality of resistance networks connect said plurality of efuse cells to said first rail and said second rail; determining a path between said first rail and said second rail offering a worst case resistance (WCR), wherein

said path passes through one of said plurality of efuse cells; and

checking whether said WCR exceeds a pre-specified value.

[c14] 14. The method of claim 13, wherein said determining further comprises:

replacing each of said plurality of efuse cells by a current source;

applying known voltages at said first rail and said second rail;

computing a voltage drop at said one terminal and said another terminal of each of said plurality of efuse cells; and

computing a first resistance value from said first rail to said one terminal of a first efuse cell by dividing the corresponding voltage drop by a magnitude of said current source, and a second resistance from said second rail to said another terminal of said first efuse cell by dividing the corresponding voltage drop by said magnitude, wherein the resistance of a path passing through said first cell equals said first resistance plus said second resistance.

[c15] 15. The method of claim 14, wherein each of said plurality of resistance equals sum of corresponding resistance offered by a first path between said first rail and said

one terminal, and corresponding resistance offered by a second path between said another terminal and said second rail.

[c16] 16. The method of claim 15, wherein said first resistance equals voltage drop across said first path divided by said current source, and said second resistance equals voltage drop across said second path divided by said current source.

[c17] 17. The method of claim 16, wherein an integrated circuit contains a plurality of said modules and a plurality of other types of module, said method further comprising:
replacing each of said plurality of modules by a corresponding WCR cell in modeling said integrated circuit.

[c18] 18. The method of claim 17, further comprising:
determining a resistance and a voltage drop to each of said WCR cells from a supply voltage; and
discarding a module if the corresponding resistance or said voltage drop exceeds a corresponding threshold.

[c19] 19. The method of claim 18, wherein determining said voltage drop comprises:
replacing each of said WCR cell by a current source having a value equaling a higher current rating in a blown or

unblown state of the WCR cell;
determining a voltage drop by analyzing a resulting circuit of said integrated circuit.

[c20] 20. The method of claim 19, wherein said voltage drop is determined by simulation.

[c21] 21. The method of claim 16, wherein said plurality of efuse cells are programmed to store a die-identifier, wherein said die-identifier identifies a die when said integrated circuit is fabricated on said die.

[c22] 22. A method of analyzing a module to determine signal characteristics of an output path of said module, wherein a design of said module is represented in the form of a data, said method comprising:
examining said data to extract an output transistor driving said output path;
determining a width of said output transistor;
detecting a pre-characterized cell containing a transistor having a width substantially matching said width of said output transistor, wherein a set of drive characteristics are associated with said pre-characterized cell;
assigning said drive characteristics of said pre-characterized cell to said output pin; and
analyzing said module to determine said signal characteristics of said output path.

[c23] 23. The method of claim 22, wherein said detecting comprises searching a library for said pre-characterized cell.

[c24] 24. The method of claim 23, wherein said drive characteristics comprise an average value, RMS value, and a peak value of a current signal on said output path.

[c25] 25. A computer readable medium carrying one or more sequences of instructions for causing a system to determine approximately whether a design of a module violates a desired criteria, said design being represented in the form of a data, wherein execution of said one or more sequences of instructions by one or more processors contained in said system causes said one or more processors to perform the actions of:
examining said data to extract a topology of said design, wherein said topology comprises a plurality of transistors, a plurality of resistors, and a plurality of paths connecting said plurality of resistors and said plurality of transistors;
generating a model of said module by replacing each of said plurality of transistors in said topology by a corresponding one of said plurality of current sources;
computing a magnitude of each of said plurality of current sources by distributing an aggregate amount of cur-

rent sunk by said module among said plurality of current sources, wherein said magnitude of each current source is treated proportionate to a corresponding width by said computing; and

analyzing said model to determine a corresponding current on each of said plurality of paths,

wherein a determination is made as to whether said design violates said desired criteria based on said corresponding current.

[c26] 26. The computer readable medium of claim 25, wherein said desired criteria comprises ensuring that a current density on each of said plurality of paths does not exceed a corresponding maximum value, said computer readable medium further comprising determining whether said corresponding current on each of said plurality of paths corresponds to a current density exceeding said corresponding maximum value.

[c27] 27. The computer readable medium of claim 26, wherein said desired criteria further comprises ensuring that a voltage drop from a supply voltage to a first node contained in said module is within a corresponding threshold value.

[c28] 28. The computer readable medium of claim 27, wherein said computing comprises treating said plurality of tran-

sistors to be connected in parallel irrespective of said topology of said design.

[c29] 29. The computer readable medium of claim 27, further comprises rejecting said module if either of said criteria is violated.

[c30] 30. The computer readable medium of claim 29, wherein said module is comprised in an integrated circuit, further comprising performing a chip-level analysis of said integrated circuit, wherein said module is substituted by said model.

[c31] 31. The computer readable medium of claim 30, wherein said analyzing of said model is performed using a simulation tool.

[c32] 32. The computer readable medium of claim 27, wherein said data representing said design is provided in the form of a layout file.

[c33] 33. The computer readable medium of claim 25, wherein said module comprises a memory module containing a memory array, said memory containing a plurality of rows, wherein said topology comprises only a subset of rows of said memory array.

[c34] 34. The computer readable medium of claim 33, wherein

said subset of rows comprises a top row, a bottom row and a middle row.

[c35] 35. The computer readable medium of claim 34, further comprising determining said top row, said bottom row and said middle row from a layout file representing said memory module, wherein said determining comprises:
examining a special layer of said layout file to determine a coordinate of a gate location of each of a plurality of transistors contained in a memory array of said memory module;
determining boundary coordinates of said memory array based on said coordinates of said gate locations; and
determining a set of transistors in each of said top row, said bottom row and said middle row according to said boundary coordinates and a height of each of bit cell contained in said memory array.

[c36] 36. The computer readable medium of claim 33, wherein said generating, said computing and said analyzing are performed in a plurality iterations, wherein a top row of said topology comprises only a top row of said memory array in a first iteration, a middle row of said topology in a second iteration and a bottom row of said memory array in a third iteration.

[c37] 37. A computer readable medium carrying one or more

sequences of instructions for causing a system to analyze a module to determine whether a plurality of efuse cells contained in a module can be programmed by applying an appropriate voltage level across each of said plurality of efuse cells, wherein one terminal of each of said plurality of efuse cells is connected to a first rail connecting to a first power supply and another terminal of each of said plurality of efuse cells is connected to a second rail connecting to a second power supply, wherein said module is represented in the form of a data, wherein execution of said one or more sequences of instructions by one or more processors contained in said system causes said one or more processors to perform the actions of:

examining said data to extract said plurality of efuse cells and a plurality of resistance networks, wherein said plurality of resistance networks connect said plurality of efuse cells to said first rail and said second rail;

determining a path between said first rail and said second rail offering a worst case resistance (WCR), wherein said path passes through one of said plurality of efuse cells; and

checking whether said WCR exceeds a pre-specified value.

[c38] 38. The computer readable medium of claim 37, wherein

said determining further comprises:

replacing each of said plurality of efuse cells by a current source;

applying known voltages at said first rail and said second rail;

computing a voltage drop at said one terminal and said another terminal of each of said plurality of efuse cells; and

computing a first resistance value from said first rail to said one terminal of a first efuse cell by dividing the corresponding voltage drop by a magnitude of said current source, and a second resistance from said second rail to said another terminal of said first efuse cell by dividing the corresponding voltage drop by said magnitude, wherein the resistance of a path passing through said first cell equals said first resistance plus said second resistance.

[c39] 39. The computer readable medium of claim 38, wherein each of said plurality of resistance equals sum of corresponding resistance offered by a first path between said first rail and said one terminal, and corresponding resistance offered by a second path between said another terminal and said second rail.

[c40] 40. The computer readable medium of claim 39, wherein said first resistance equals voltage drop across said first

path divided by said current source, and said second resistance equals voltage drop across said second path divided by said current source.

[c41] 41. The computer readable medium of claim 40, wherein an integrated circuit contains a plurality of said modules and a plurality of other types of module, said computer readable medium further comprising:
replacing each of said plurality of modules by a corresponding WCR cell in modeling said integrated circuit.

[c42] 42. The computer readable medium of claim 41, further comprising:
determining a resistance and a voltage drop to each of said WCR cells from a supply voltage; and
discarding a module if the corresponding resistance or said voltage drop exceeds a corresponding threshold.

[c43] 43. The computer readable medium of claim 42, wherein determining said voltage drop comprises:
replacing each of said WCR cell by a current source having a value equaling a higher current rating in a blown or unblown state of the WCR cell;
determining a voltage drop by analyzing a resulting circuit of said integrated circuit.

[c44] 44. The computer readable medium of claim 43, wherein

said voltage drop is determined by simulation.

[c45] 45. The computer readable medium of claim 40, wherein said plurality of efuse cells are programmed to store a die-identifier, wherein said die-identifier identifies a die when said integrated circuit is fabricated on said die.

[c46] 46. A computer readable medium carrying one or more sequences of instructions for causing a system to analyze a module to determine signal characteristics of an output path of said module, wherein a design of said module is represented in the form of a data, wherein execution of said one or more sequences of instructions by one or more processors contained in said system causes said one or more processors to perform the actions of:
examining said data to extract an output transistor driving said output path;
determining a width of said output transistor;
detecting a pre-characterized cell containing a transistor having a width substantially matching said width of said output transistor, wherein a set of drive characteristics are associated with said pre-characterized cell;
assigning said drive characteristics of said pre-characterized cell to said output pin; and
analyzing said module to determine said signal characteristics of said output path.

[c47] 47. The computer readable medium of claim 46, wherein said detecting comprises searching a library for said pre-characterized cell.

[c48] 48. The computer readable medium of claim 47, wherein said drive characteristics comprise an average value, RMS value, and a peak value of a current signal on said output path.